

ABSTRACT OF THE DISCLOSURE

A semiconductor device with a surge protection circuit includes a surge protection circuit electrically connected to a signal input terminal and having an npn transistor and an npn transistor. The semiconductor device is configured such that the npn transistor is more susceptible to breakdown than the npn transistor, by implementing such a configuration that a narrowest region of a base of the npn transistor has a width different from that of a narrowest region of a base of the npn transistor. Thus, a semiconductor device with a surge protection circuit attaining a normal operation can be obtained.

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